



RESEARCH DEPARTMENT



REPORT

An experimental digital picture store

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AN EXPERIMENTAL DIGITAL PICTURE STORE

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Summary

This Report outlines the design of a 3.6 Mbit digital store suitable for television signals sampled at frequencies of up to approximately 3 x colour sub-carrier frequency. The design had to be flexible in order to meet a wide-range of requirements involving this type of storage. The final machine met its target specification and incorporated a comprehensive store control system which greatly assists the user in the management of this large store. The store was constructed in two identical halves which could be used for two independent investigations, provided that each required no more than the capacity corresponding to one television field. The completed store could also be used for other applications involving much lower sampling frequencies, such as those used for digital audio signals.

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1. Glossary of terms

address	A number specifying the location of data within a storage assembly.
back plane	The mechanical assembly carrying the interconnections between several printed-circuit boards.
dynamic (memory)	A device whose storage characteristic is a function of time. Usually, the stored data decays and must be regenerated within a finite time.
industry standard	A component which is more or less widely adopted by the branch of industry concerned and is made to a common specification by several manufacturers.
Pseudo-random sequence generator	A device which generates a well-defined and repetitive sequence of near random numbers.
random access	A memory in which the writing and reading locations may be used in any order.
read access time	The time which must elapse before any particular data can be read out from a store.
real-time	(processing) The processing of a function or variable which takes place as that function or variable occurs. That is, no compression or expansion of the time-scale is permitted.
static (memory)	A device whose storage characteristic is not a function of time. The data remains unaltered so long as the power is supplied, and sometimes, even after the power is disconnected.
wire-NAND	The Boolean logic function NAND achieved by external wiring between the outputs of semiconductor logic functions rather than by the more usual internal connections.

2. Introduction

Since the advent of relatively cheap digital storage devices it has become feasible to build a digital store with

a capacity of one digitally-coded television picture, and for input and output bit-rates corresponding to real-time television signals. Such a store has been built, having a capacity of approximately 3.6 Mbits and a maximum data transfer rate of greater than 106 Mbit.s^{-1} at both input and output.

A number of areas of work within Research Department require storage of this kind.

3. Store requirements

The store was required to have a word capacity at least equivalent to the active area of the picture, that is 576 lines of 692 samples, the word length being 8 bits. The maximum data transfer rate had to exceed $13.5 \text{ M word.s}^{-1}$.

In practice, because of the arrangement of generally available storage elements a target of 592 lines of 768 words was more convenient. A design upper frequency limit of $13.5 \text{ M word.s}^{-1}$ gave some margin on the operating speed.

To meet the requirements of a large variety of applications, it was necessary to incorporate a wide range of facilities in the final design. The operation and control of the store also had to be largely self-contained in order to avoid the need for different user groups to design and construct complex store-control equipment. This feature makes the use of the store by such groups relatively economical, as each group has only to concentrate on the problems peculiar to its own work and not on the internal design of the store.

The facilities eventually decided were as follows:

1. The store to be constructed in two autonomous halves so that two different groups could each use one half, provided that each group required only 1 field (288 lines) of storage.
2. The input and output to be asynchronous, in relation to each other, at least within the limits imposed by picture-source synchronization and field-store standards-conversion requirements.
3. Any line of data stored to be randomly accessible, so that the order of line-length blocks of data at the output need not be the same as that in which the data had been written into the store.
4. Two independent "read" outputs to be available from each half of the store making a total of four outputs when the two halves are used together. This arrangement is convenient for work such as

- standards conversion where interpolation between several lines is necessary.
- 5. The reading of data from the store to be destructive if the output data is required once only or non-destructive if it will be required again.
- 6. For those cases where only a very simple storage programme is required, provision to be made in the main body of each half for a "LOCAL PROGRAMME" board to be inserted. This board location has connected to it all of the connections which are normally made to the rear panel (Fig. 4), the changeover being effected by operation of the LOCAL/REMOTE switch on the front panel. When selected, the LOCAL PROGRAMME board can be arranged by the user to provide all of the addresses and waveforms required by the store for a simple programme. This facility is to simplify the use of the store at a distance using analogue input and output connections made to a "codec" situated at the store. If the programme generator is external to the main body of the store it is not practicable to operate the store in the normal way using long wires from a remote point because of the very large number of connections (from 43 up to 70) which must be made.

In addition to these facilities, four requirements were imposed on the design. First, the store must be transportable as it will not always be practicable or convenient for the users to transport their equipment to it or to use it remotely.

Secondly, with such a complicated piece of equipment, it was necessary to incorporate a comprehensive self-checking arrangement in order to locate faults.

Thirdly, the store must operate over a wide range of clock frequencies. For applications such as those in which a single field or picture of television is "grabbed" for subsequent computer processing or where a single field or picture is slowly built up for later repetitive real-time replay, a clock speed range in excess of a hundred to one must be accommodated. This also permits the store to be used for other purposes such as digital audio storage.

The fourth requirement was that the store operation must be effectively "static" although employing "dynamic" devices. This means that the data must not be corrupted by a long (several hours) storage time.

4. Implementations

4.1. Store board

The basic storage element was a 256 word x 4 bit shift register, type 1402A. This device is made by many integrated circuit manufacturers as an "industry standard". Supplies of this device were easy to obtain and prices very low for the quantity needed (nearly 4000). Because of the requirement for random access, at least on a line by

line basis, some consideration was given to designing the store around random access memories (RAMs). At the time when the basic outline of the complete store was finalized, even those types of RAMs which had been in production for some time cost about four times the price of the shift registers. This factor would have doubled the component cost of the complete store and so the decision was taken to employ shift registers.

These shift registers are "dynamic" devices which means that if they are not clocked at frequency above a certain minimum, the data becomes corrupted. Therefore it is necessary to provide a recirculating loop from the output of each device or group of devices back to the input. The data can then be clocked around the loop whenever the device is not required by the writing or reading process. This recirculating loop involves additional logic and it was necessary to find the optimum size of the loop. If it were too small then a larger amount of logic would be required. If it were too large then the access time to the data within the loop would become large for the following reason; before reading out can begin, the data must be shifted into such a position that the first word written in is the first word read out. A loop containing two shift registers in tandem was finally chosen as the optimum. Fig. 1 shows the basic element of storage from which the store board was assembled; this element contains two 256-bit blocks of storage. By having two access points in the loop, the read access time is halved without the complexity of additional recirculate logic. The two output busbars are wire-NAND connected for economy and, together with a two-position multiplex system for the read address, allow two independent lines to be read out simultaneously from the main store assembly, irrespective of where those two lines are stored. Four such storage elements are combined to provide 4-bit words and the 4-bit unit is repeated 8 times on each storage board. This results in 16 K bits of storage/board.

The shift registers have an upper data rate of 5 M bits s^{-1} . In order to be able to handle data at up to $13.5 \text{ M words s}^{-1}$ three store boards must be multiplexed together. Further three 256-bit storage blocks provide a total of 768 bits and, when arranged with another such set of three boards so as to make-up the word length to 8 bits, gives a storage unit of 768 words x 8 bits. This is the basic block of storage into which the data is divided and corresponds to the active line and burst of 625/50 PAL television sampled at around 13.3 MHz. Thus the data representing this part of a television line is split up amongst 6 different storage boards. The complete set of 6 boards has a combined capacity equivalent to 16 television lines.

Each store board also contains a pair of discrete clock drivers. Because the clock input connection to the shift registers is capacitive and totals about 1200 pF per board, a large clock-drive current is necessary to achieve the speed required. The current pulse generated has a peak amplitude of 2.2 A and a width of 35 ns. Discrete clock drivers were chosen because they were cheaper and had a better performance than the integrated types.

Address decoders on each store board decode three

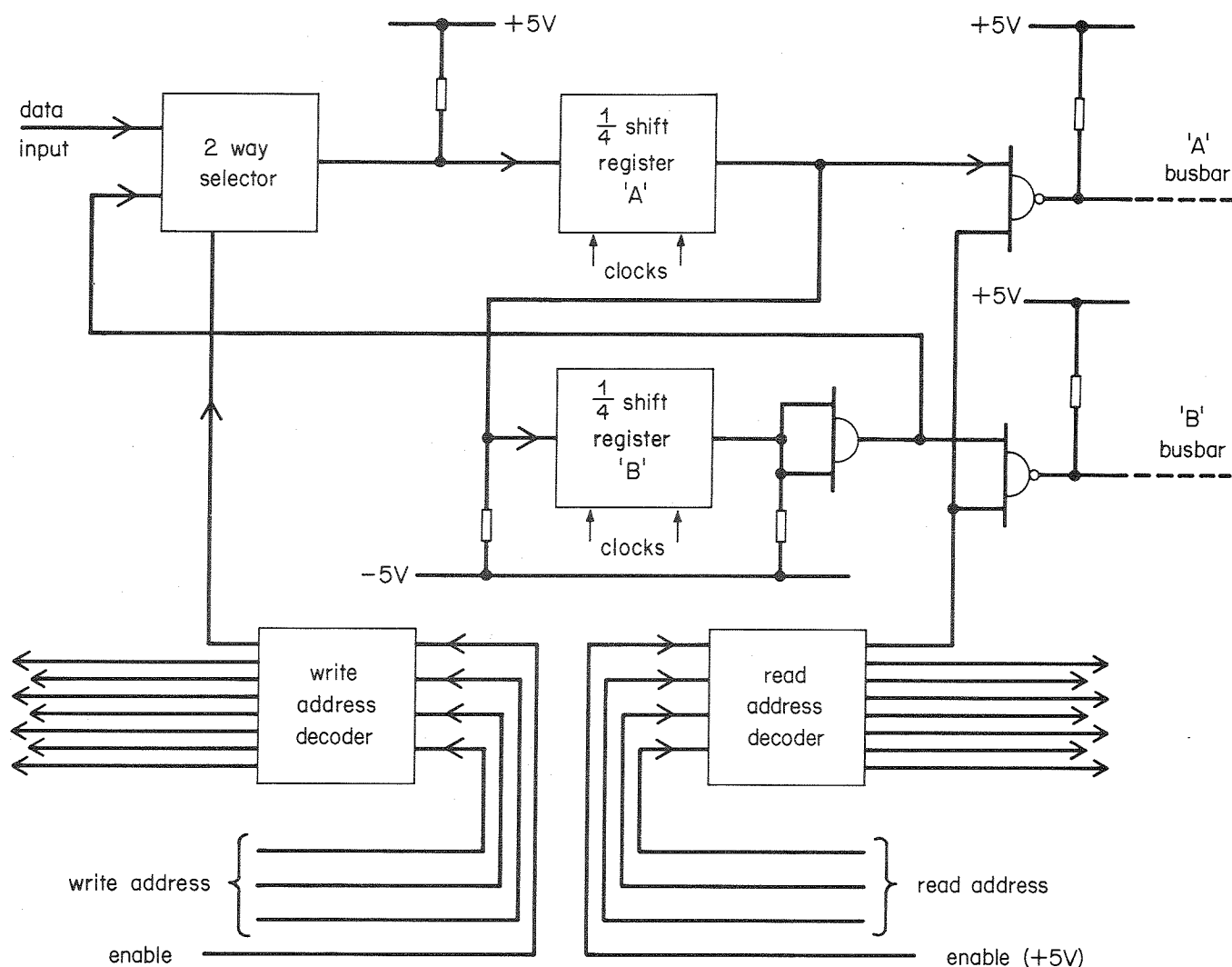


Fig. 1 - Basic storage element

bits of the address to select one of the 8 groups of shift registers for reading and writing.

4.2. Main store assembly

The main part of each half of the store consists of 114 store boards arranged in 6 racks of 19 boards each. The group of six boards which make up the 16 blocks of storage as described in Section 4.1. are arranged in a vertical column. 19 such columns give a total storage capacity of 304 blocks; this includes one column more than is necessary in theory, because of the requirement to "phase-up"* each column before reading or writing.

Each column has a COLUMN CONTROL BOARD associated with it. This board contains a clock counter that keeps track of the phase of the data in the store

boards. By having a separate board dedicated to this function, the amount of logic on each store board can be kept to a minimum and the number of clock counters reduced by a factor of 6. In fact each column control board contains the control logic for two columns, so that only 8 complete and 3 half boards are required in each half of the store. The column control board also contains logic for driving the WRITE ENABLE inputs and for the multiplexing of the READ DATA outputs.

Each row of 19 boards has a ROW CONTROL BOARD associated with it. The row control board contains logic for demultiplexing the input data, for multiplexing the output data, and for driving the horizontal data and address busbars that run the length of the row.

By using this orthogonal arrangement, the maximum length of the connections between the various parts of the store can be kept to a minimum. In fact, the longest connection within the main store assembly is only about 0.60 m. This, together with the fact that the whole back plane of the main store assembly was designed with a continuous "earth plane" (an area of 0.42 x 1.25 m), means

* The necessity to phase-up the columns arises because the recirculation of the data takes place at less than the full clock rate, in order to save power. This point will be covered in a later section.

that signals can be provided and accepted by ordinary logic elements; no line drivers or receivers are required. The vertical connections from the column control board to its store boards are made by a plug and socket arrangement. In this way, a complete row can be removed by unplugging, the number of soldered joints being relatively small. Thus, in the event of a failure in a section of the back plane, it can be replaced easily. It also meant that the majority of the vertical wiring could be done on the bench rather than on the main frame. This gave a significant saving in the effort required for the assembly of the 1600 joints involved.

4.3. The control system

What has been described so far is a straight-forward storage assembly, in which a given address corresponds to a physical location (machine code). If this were to be the mode of operation as far as the user is concerned, he would have to keep account of the location in which every block of data was stored and which locations were available for new data. A comprehensive control system was therefore provided so that these matters can be dealt with by the store itself (Fig. 2). The principle of operation is that new data is written into one of the empty locations and the store control keeps a record of which locations are full. A record is also kept of which physical locations correspond to the addresses provided by the user. In this way the users' addresses function merely as labels and bear no relationship to the physical location of the data.

The two parts of the control system which carry out this function are the SCRATCHPAD and the ASSOCIATIVE MEMORY. The scratchpad contains a 768 x 1 bit RAM and the logic to carry out search and update functions in this RAM. The first 608 locations in this RAM correspond to the 608 lines of storage in the main store. A logic 1 in any location indicates that the corresponding store location contains wanted data. At the beginning of every block a search is carried out, starting at address 0 and progressing upward until an empty

location, logic 0, is found. Because of the requirements for write and read phase-up periods, and because the information is stored in two block units, a number of conditions are imposed on the availability of the store location. The first vacant store address may not in fact be available because of these limitations and, if so, the search must continue until a valid vacant address is found. The vacant address is then transferred to the WRITE STACK (see Section 4.4.), at which time the appropriate column can be phased-up ready for the input data.

When the input data is written into the store, the same address is sent to the associative memory where it is stored in a 1 k x 10 bit RAM against the users label.

To recall the data, the user supplies his original label to the READ ADDRESS input. This label interrogates the associative memory to obtain the machine-code address and thus the location of the required data.

If no free location is found by the search routine then the store is judged to be full and a front panel lamp is illuminated to indicate the "store-full" condition.

Each half of the store has sufficient logic to control the whole store so that when the two halves are joined together each half contains all of the information about the addresses. Thus the two halves can work either separately or together, without the need for a large number of address connections between them. It also means that both halves are identical except for one or two permanently wired links within the control system. Those links define the most significant bit of the above addresses.

4.4. Recirculation and the read and write stacks

Because the shift-registers are dynamic devices, they must still be clocked at some minimum clock rate when data is stored and not being read out. During this time, the data goes round the recirculating loop and back into the shift-register. The recirculation clock rate can be much

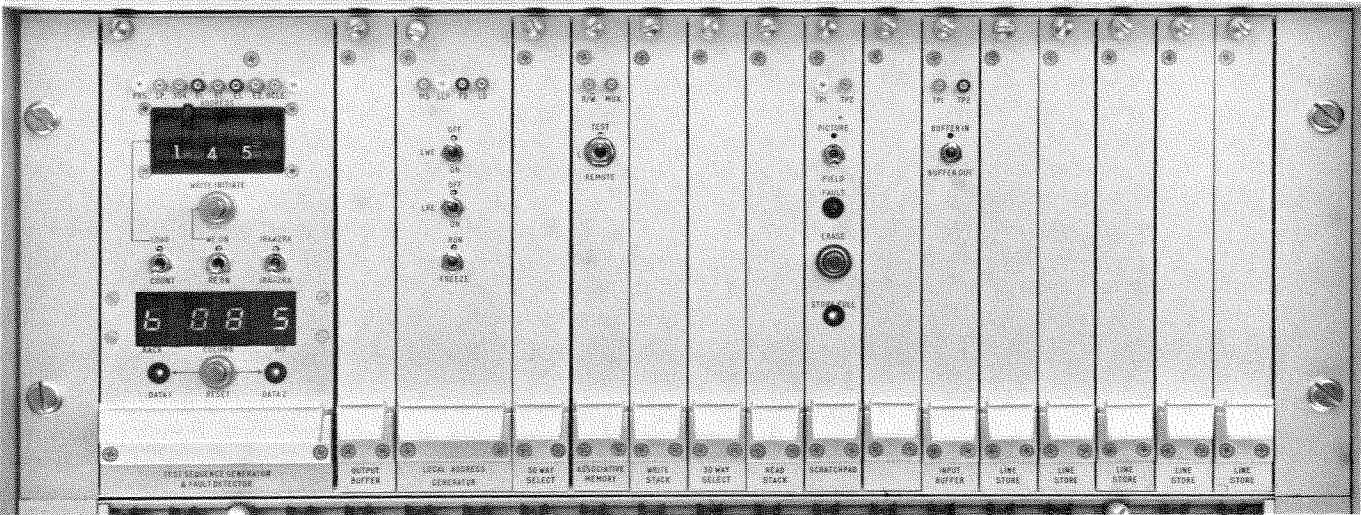


Fig. 2 - Store control system

less than that used for writing, which considerably reduces the power consumption of the device. In practice, the recirculating clock rate is 1/16 of the normal shift-register clock rate. This reduces the power consumption of the whole store from about 6.5 KW (at 13 M sample s^{-1}) to 3.3 KW in the worst case, or about 3.0 KW for fairly simple applications. This leads to a very considerable simplification of both the power supplies and the cooling arrangements.

The need for read and write stacks follows as a direct consequence of this recirculation. Fig. 1 shows that, because of the arrangement by which writing can only take place at the beginning of two blocks of data, up to two complete block periods may be required to get the storage unit into a suitable phase; thus writing cannot take place until the third period. Therefore the write address must be available for a total of three block periods after the vacancy has been found by the scratchpad. The write stack stores the write address as required.

The read address stack is one block longer than the write address stack, as the read address must be available during the search for the next write address. This arises because of some restrictions on reading from a column during the write phase-up period.

Thus the user's write address and write enable are required three block periods before the data is written into store, and the user's read addresses and read enables are required four block periods before the data is available at the output.

4.5. Input buffer

The input buffer is required for any application in which the read and the write blocks are not synchronous. It was not convenient to design the main store for asynchronous operation so the input buffer deals with the asynchronism and transfers the input data from write clock and block timing to read clock and block timing, the main body of the store thus operates entirely according to read clock and block timing. So that no data is lost, the capacity of the buffer must be sufficient for the worst probable application. The capacity provided, consisting of 5 x 768 words x 8 bits, is sufficient to deal with 525/60 to 625/50 standards conversion.

4.6. Output buffer

The data from the shift registers is clocked out 180 ns after the input clock timings and additional delays in the read path increase this figure somewhat. The output buffer effectively removes this inconvenient time delay and restores the data timing approximately to that of the read clock input. This makes the overall delay of the read data-output into an integral and constant number of clock pulses plus a small delay of a fraction of a clock pulse, even at the highest clock frequency.

4.7. Test facilities

With such a large piece of equipment it is essential that a self-checking facility be incorporated. This consists

of a block-length, pseudo-random sequence generator, the signal from which is written into every store location once only. Switching to the read mode, all the store locations are addressed in turn and their output data compared with the sequence generator. Any discrepancy stops the address counters at the address containing the fault. Since the test facility works in machine-code, the address can be decoded to indicate both the faulty store board and also that particular bit of the data which was affected by the fault. This information is displayed on numerical indicators on the front panel. A further operation of switches on the front panel and within the test generator can locate the fault more exactly (Fig. 3).

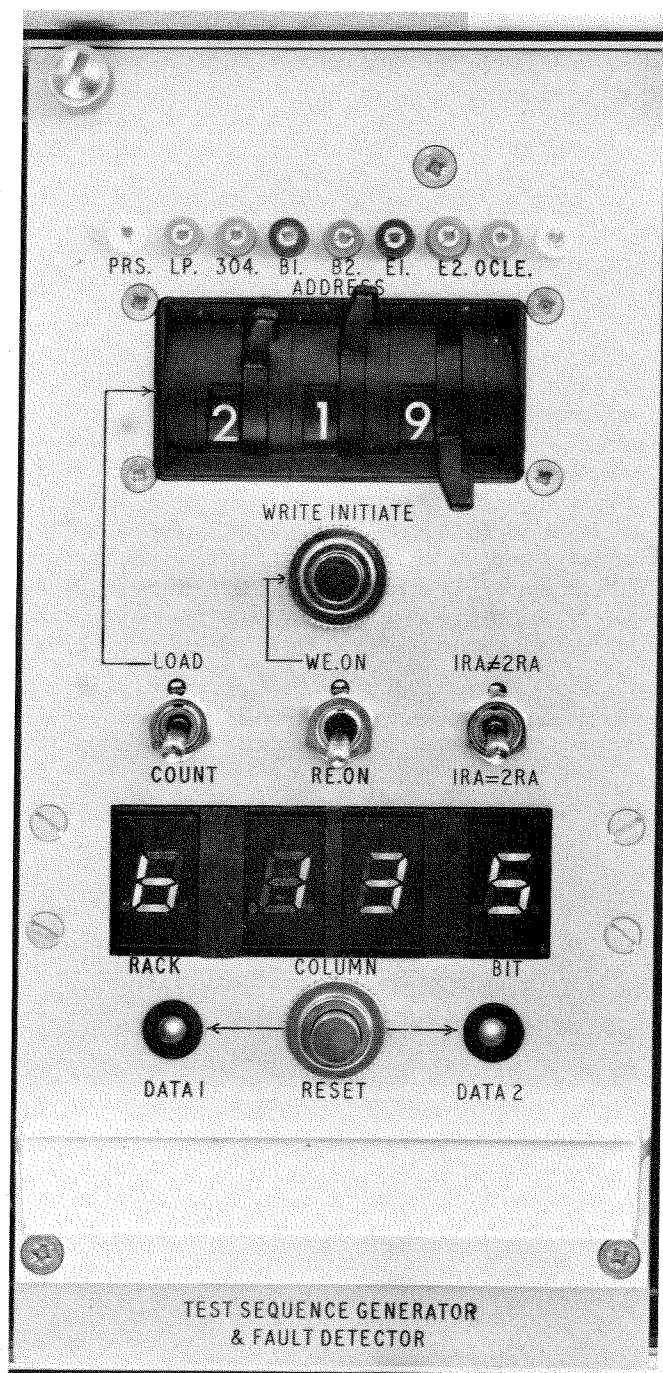


Fig. 3 - Test sequence generator

4.8. Power supplies and cooling arrangements

Each half of the store requires power supplies of 120A at +5V, 60A at -5V and 8A at -11V relative to earth. This power is supplied by five switching-regulated power supplies arranged in a series - parallel configuration. To limit the damage which might occur if one of them fails, the +5V rail is common to all the power supplies and -10V and -16V are generated relative to it. To control the inrush current at switch-on, the 240V AC is first applied, by a relay, through a low value resistor. The resistor is shorted out by a second relay when the output voltages become established.

The power is distributed by a number of busbars of large cross-section, so as to minimize the voltage drops between the top and the bottom of the store and to reduce circulating currents. Remote sensing is not employed as the voltage drops are small and serious damage could occur if the remote sensing became disconnected.

With such large capacity power supplies, serious damage could also occur if any power supply were inadvertently short-circuited. In particular the +5V power is the most widely distributed and has the largest current supplying capability. A protection scheme was incorporated into the main store assembly consisting of a current-sensing coil containing a reed switch in series with the +5V connection to every board. If any board takes more than about 3A, the reed switch closes which, in turn, triggers two thyristors. One thyristor is connected directly across the supply busbars and reduces the voltage to about 1 volt in less than 1 ms. The second thyristor short-circuits the mains relay coil, thus disconnecting the power.* All the power supply voltages are monitored and

* The speed of this reaction is such that during tests a 1 amp fast-blow fuse did not rupture when used to short circuit the 120A supply.

fitted with upper and lower limit indicators on the front panel.

A cooling fan is fitted near the bottom of each half of the store to maintain an upward flow of cooling air through the equipment. Some of this air is bled off downwards to provide cooling for the power supplies.

4.9. Inputs and outputs

To enter data into the store without the input buffer requires inputs of write data, write clock, write line-pulse (to define the beginning of the data block), write address and write enable. Any ten-bit binary number is a valid address. If the input buffer is used then the read line-pulse and the read clock must also be supplied.

To obtain output data requires inputs of read line-pulse, read clock and one or two read addresses, read enables and destructive/non-destructive read control signals depending on whether one or both of the data outputs are being used. In addition, a single link is provided between the connection panel and the local-programme board position so that synchronising pulses or another control waveform can be supplied by the user to the local programme generator.

All these connections are made to the rear panel (Fig. 4) where they are received or sent as appropriate by "standard timing" circuits.* These enable multiway connections of up to about 2 metres, using miniature

* "Standard timing" is a specification now adopted by BBC Research Department which lays down nominal data/clock timings and includes provisions which will allow the highest probability of a satisfactory interconnection between any two digital-television processing units, allowing for worst-case timing tolerances. A long period is allowed for the signal transients to die away before the signal is reclocked; this is advantageous when long connecting cables are used.

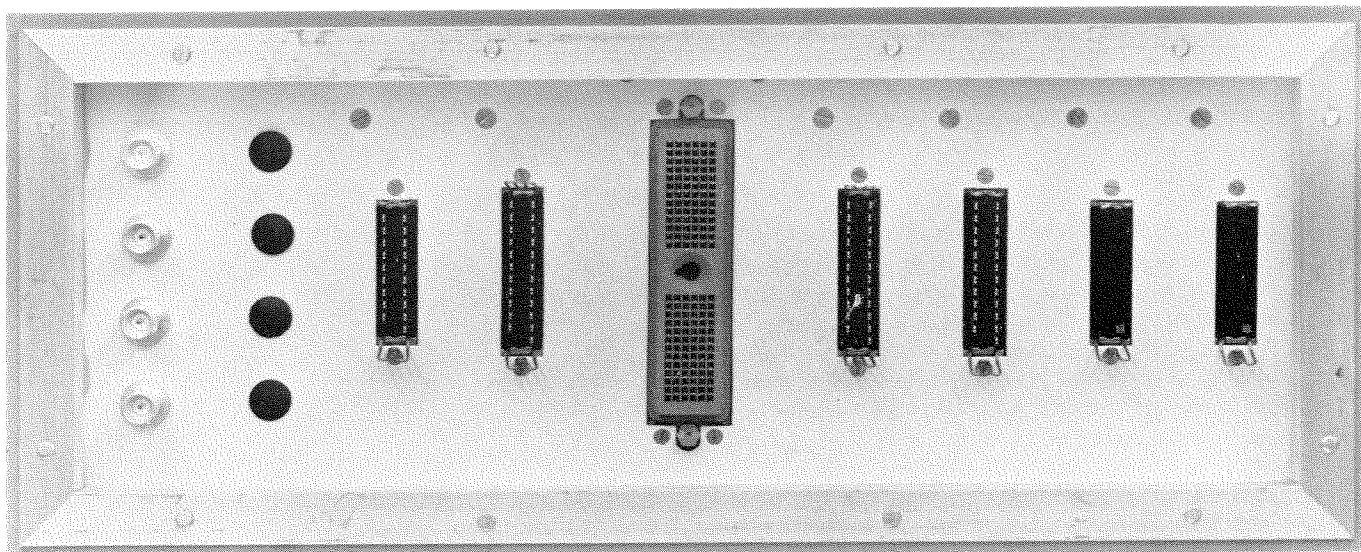


Fig. 4 - Rear connection panel

25-way multicore cable, to be made between the store and the users' equipment.

When the two halves of the store are being used together, a single, multiway interconnecting cable provides all the necessary signals between the two halves. The user has only to make connections to one half. In fact, the interconnection is such that the inputs may be connected to one half and the outputs taken from the other half.

5. The completed store

5.1. Characteristics

The completed store meets all of the requirements laid down in Section 3. It weighs approximately 500 Kgm and contains about 3700 storage devices and about 11,000 other pieces of TTL logic.

A specification of the store is available, and a handbook has been prepared which contains all of the circuit diagrams and an outline of the operation of each circuit board sufficient for maintenance purposes.

Fig. 5 shows a photograph of the store.

5.2. Reliability

With such a large logic system, failures are to be expected fairly frequently. A calculation of the expected reliability using such figures as are available is contained in the handbook; it predicts a mean time between failures of about 300 hours. In practice, the initial failure-rate was much higher than this, but after a "burn-in" period of several months, very few failures occurred.

The power supplies were especially unreliable and measurements showed that they were operating near to their temperature limit. Additional cooling was provided to reduce the temperature of the power supplies by 10°C. Although this modification had only been in operation for a few months, the absence of further failures suggests that the problem has now been overcome.

6. Conclusions and future outlook

The experimental picture store is achieving all the design requirements when handling one television picture

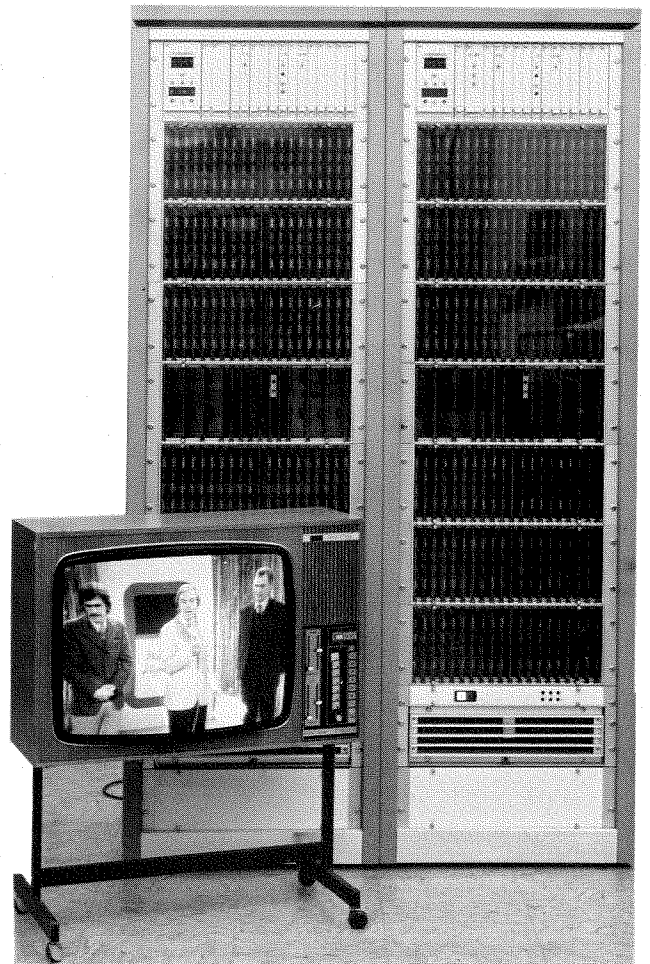


Fig. 5 - The completed picture store

at the data-rate necessary for real-time applications.

Since the work was started the storage-device situation has changed, and it would not now be considered reasonable to design a flexible store using shift-registers. The price and availability of large random-access devices implies that any future store of this kind would probably be designed using devices such as 4 Kbit or the 16 Kbit random-access memories.

In addition, for any one fixed application such a flexible and comprehensive specification would not be necessary and the control system would be much simplified or even eliminated altogether.